

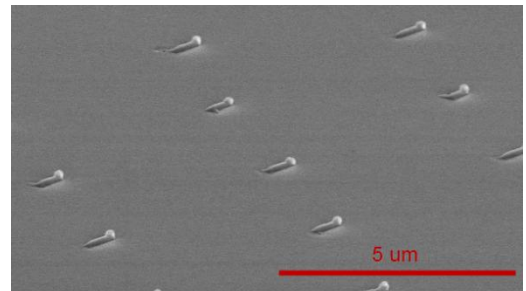
NANO HOUR

Wednesday, March 16, 2011 3:00 pm
Beckman Institute - Room 3269

Towards Planar GaAs Nanowire Array FETs: Direction and Doping Control

Ryan Dowdy, Electrical and Computer Engineering
Graduate Student with Professor Xiuling Li

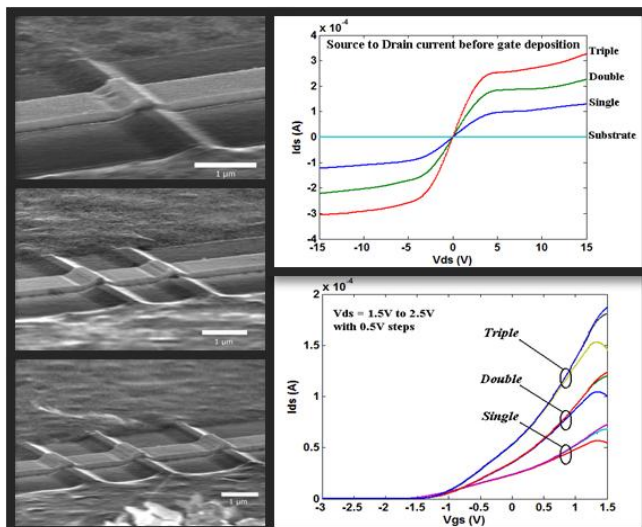
Nanowires have proved themselves to be a robust and versatile nanotechnology building block. While a myriad of electrical and optical devices have been demonstrated, there is still an issue of integrating nanowires with traditional planar devices. Planar GaAs Nanowires, which epitaxially grow along the surface, are presented as a possible solution to this problem. Planar GaAs nanowires are self aligned, have a naturally low defect density with smooth and well defined crystalline facets.



Through the use of various substrates, we present additional control over planar nanowire growth directions with visual and X-Ray analysis. We are able to achieve isodirectional and uniform planar GaAs nanowire arrays. Additionally, we are able to perturb the growth of the planar nanowire and achieve axial twinning superlattice which potentially has additional desired electrical and optical properties. This work lays the foundation for self-aligned, site-controlled, in situ epitaxially grown planar nanowire arrays for practical applications in nanoelectronics.

Multiple-channel Planar III-V Nanowire High Electron Mobility Transistor

Xin Miao, Electrical and Computer Engineering
Graduate Student with Professor Professor Xiuling Li



We have demonstrated the first planar III-V nanowire (NW) based high electron mobility transistor (NW-HEMT) with self-assembled $\langle 110 \rangle$ GaAs NW as the conducting channel capped with Si-doped AlGaAs. The NW-HEMT structure is grown monolithically in a MOCVD reactor and fabricated using conventional optical lithography. The device can be tuned to work either in depletion or enhancement mode by adjusting the AlGaAs thickness and doping. A single-channel depletion mode GaAs NW-HEMT with 940 nm gate length shows a Subthreshold slope of 134 mV/dec, peak gm of 95 mS/mm (at 2.5V drain bias), and I_{ON}/I_{OFF} ratio of 10^4 . NW-HEMTs with multiple NWs as channel have shown that source drain current scales with the number of NW channels very well, verifying the high uniformity of our NW-HEMT structure and the feasibility of NW array based FETs for practical applications.

Coffee and cookies will be served

<http://nanohour.beckman.illinois.edu>