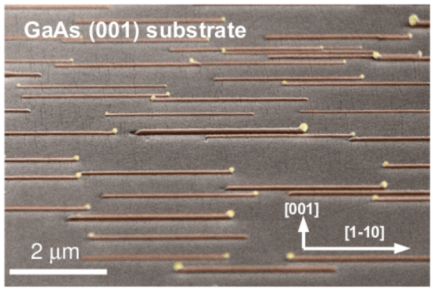
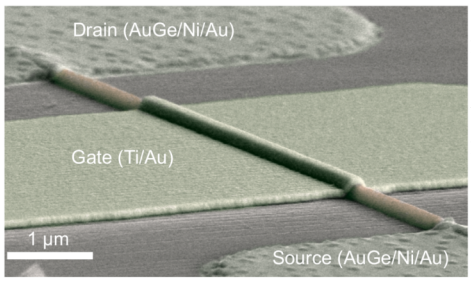
NANOHOUR

Wednesday, November 4, 2009 3:00 pm
Beckman Institute - Room 3269

Planar III-V Nanowire for Integrated Bottom-up Nanoelectronics and Nanophotonics

Seth Fortuna – Electrical and Computer Engineering



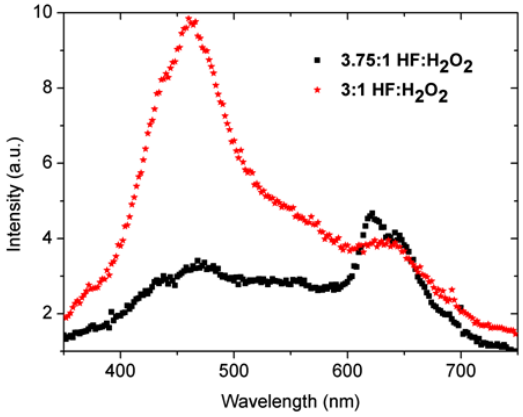


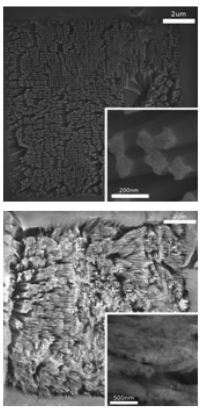
Metal-catalyzed semiconductor nanowires have garnered much attention over the past several years as a promising nanotechnology building block. III-V semiconductor nanowires are of particular interest because of their direct bandgap, high carrier mobility, and ability to form heterojunctions. However, the abundance of stacking faults has been widely reported and wafer-scale integration of nanowires with current planar processing technology remains a challenge for the commonly grown out-of-plane nanowire geometry. Recently, we demonstrated a controlled growth method of self-aligned and low-defect <110> III-V planar nanowires on (001) substrates. III-V planar nanowires grow self-aligned in the [1-10] or [-110] directions laterally and epitaxially on the surface and thus stay effectively pinned to the (001) substrate during growth. Through growth on a sacrificial layer, III-V planar nanowires can be transfer-printed to other substrates while maintaining position and alignment. The planar geometry and low-level of crystal defects along with the transfer-print capability could potentially lead to highly integrated III-V nanoelectronics and nanophotonics. In this talk, the controlled growth of III-V planar nanowires and transfer-print process along with our recent results on a planar nanowire-based GaAs MESFET will be presented.

Non-lithographic Patterning and Metal-Assisted Chemical Etching for Manufacturing of Tunable Light-Emitting Silicon Nanowire Arrays

Winston Chern – Electrical and Computer Engineering

Semiconductor nanowires have potential applications in energy storage and conversion by engineering the geometry and optical properties. We report a novel top-down fabrication method for the formation of silicon nanostructures with defined morphological and optical properties. This method combines superionic solid state stamping (*S4*) patterning with metal assisted chemical etching (*MacEtch*), producing silicon nanowire arrays with strong emission in the entire visible wavelength range at room temperature in a manufacturable fashion. The etching conditions can be controlled to tune the wavelength and intensity of the visible emission, which is attributed to surface features rather than the nanowire body with dimensions far beyond the quantum confinement size threshold. Through the removal of remaining Ag pattern and redeposition of Ag films on the Si nanowires, plasmonic enhancement of the blue emission has also been demonstrated.





Coffee and Cookies will be served

http://nanohour.beckman.uiuc.edu